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EXAMINER	
LEE, CHRISTOPHER E	
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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/044,401	DELANO, ERIC R.	
	Examiner	Art Unit	
	Christopher E. Lee	2112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-17 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-17 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 2.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The following guidelines illustrate the preferred layout for the specification of a utility application. These guidelines are suggested for the applicant's use.

Arrangement of the Specification

As provided in 37 CFR 1.77(b), the specification of a utility application should include the following sections in order. Each of the lettered items should appear in upper case, without underlining or bold type, as a section heading. If no text follows the section heading, the phrase "Not Applicable" should follow the section heading:

(a) TITLE OF THE INVENTION.
(b) CROSS-REFERENCE TO RELATED APPLICATIONS.
(c) STATEMENT REGARDING FEDERALLY SPONSORED RESEARCH OR DEVELOPMENT.
(d) INCORPORATION-BY-REFERENCE OF MATERIAL SUBMITTED ON A COMPACT DISC (See 37 CFR 1.52(e)(5) and MPEP 608.05. Computer program listings (37 CFR 1.96(c)), "Sequence Listings" (37 CFR 1.821(c)), and tables having more than 50 pages of text are permitted to be submitted on compact discs.) or
REFERENCE TO A "MICROFICHE APPENDIX" (See MPEP § 608.05(a). "Microfiche Appendices" were accepted by the Office until March 1, 2001.)
(e) BACKGROUND OF THE INVENTION.
(1) Field of the Invention.
(2) Description of Related Art including information disclosed under 37 CFR 1.97 and 1.98.
(f) BRIEF SUMMARY OF THE INVENTION.
(g) BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWING(S).
(h) DETAILED DESCRIPTION OF THE INVENTION.
(i) CLAIM OR CLAIMS (commencing on a separate sheet).
(j) ABSTRACT OF THE DISCLOSURE (commencing on a separate sheet).
(k) SEQUENCE LISTING (See MPEP § 2424 and 37 CFR 1.821-1.825. A "Sequence Listing" is required on paper if the application discloses a nucleotide or amino acid sequence as defined in 37 CFR 1.821(a) and if the required "Sequence Listing" is not submitted as an electronic document on compact disc).

In this case, the text disclosure does not have a title (e) BACKGROUND OF THE INVENTION.

The Office suggests the above preferred layout for the specification of a utility application.

Claim Objections

2. Claim 17 is objected to because of the following informalities: Substitute "to::" in line 3 by--to:--. Appropriate correction is required.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 12 and 15-17 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The claims 12, 16 and 17 recite the limitation "the destination output port" in line 10 of the claim 12, in line 13 of the claim 16, and in line 5 of the claim 17, respectively. There is insufficient antecedent basis for this limitation in those respective claim. Therefore, the term "the destination output port" could be considered as --a destination output port-- since it is not clearly defined in the claims.

The claim 15 recites the limitation "the width of the input port" and "the width of the output port" in lines 3-4. There are insufficient antecedent basis for these limitations in the claim. Therefore, the term "the width of the input port" and "the width of the output port" could be considered as --a width of the input port-- and --a width of the output port--, respectively, since those are not clearly defined in the claims.

The claim 15 recites the limitation "the processed data" in line 5. There is insufficient antecedent basis for this limitation in the claim. Therefore, the term "the processed data" could be considered as --a processed data-- since it is not clearly defined in the claims.

The claim 17 recites the limitation "the crossbar control data" in line 9. There is insufficient antecedent basis for this limitation in the claim. Therefore, the term "the crossbar control data" could be considered as --a crossbar control data-- since it is not clearly defined in the claims.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1, 3, 6-8, 11-13 and 15 are rejected under 35 U.S.C. 102(b) as being anticipated by Yokoyama [JP 411296473 A; cited by the Applicant].

Referring to claim 1, Yokoyama discloses a crossbar (i.e., crossbar switching system in Fig. 1) for providing connections between a plurality of ports (e.g., DA I/O Board #1-#4 in Fig. 1) and a plurality of system agents (e.g., Processor Boards #1-#2, and Memory Boards #1-#2 in Fig. 1) via a processing system (i.e., Crossbar Switch 5, Crossbar Switch I/O ports 6, Address Controller 8 and Data division 7 in Fig. 1) comprising: a plurality of ports (i.e., ports for Processor Boards #1-#2, Memory Boards #1-#2, and DA I/O Board #1-#4 in Fig. 1), each port capable of being an input port customized (See Figs. 3 and 11; i.e., SW#2 being set '1' and SW#3 being set '1' make the port customize as an input port in Fig. 3) for receiving data from a source agent (i.e., receiving data from Processor Board in Fig. 1) and an output port customized (See Figs. 3 and 11; i.e., SW#2 being set '0' and SW#3 being set '0' make the port customize as an output port in Fig. 3) for transferring data to a destination agent (i.e., transferring data to DA I/O port in Fig. 1); and, crossbar control data (i.e., discernment bits Sa and Sb, and Address in Fig. 2) for specifying crossbar control information (i.e., Crossbar Switching control information) for transferring data from an input port to an output port (See Figs. 25-38) having different port configurations (i.e., having 128 bit and 256 bit port configurations; See Paragraphs [0148], [0149], [0154], and [0155], as an example).

Referring to claim 3, Yokoyama teaches at least one register (i.e., memory A 61-b1 and memory B 61c-1 in Fig. 9) on each input port and each said output port for storing data in

memory (i.e., storing configuration environment of the crossbar switch in the memory A, and partner's board name and port number in the memory B; See paragraphs [0076]-[0077]).

Referring to claim 6, Yokoyama teaches an input port and an output port (e.g., ports for Processor Boards #1-#2 and Memory Boards #1-#2 in Fig. 1 configured as input ports, such that SW#2 being set '1' and SW#3 being set '1' making the port configure as an input port, and ports for DA I/O Board #1-#4 in Fig. 1 configured as output ports, such that SW#2 being set '0' and SW#3 being set '0' making the port configure as an output port according to Figs. 3 and 11) of at least one of said plurality of ports (e.g., ports for Processor Boards #1-#2 and Memory Boards #1-#2 in Fig. 1) are customized to have different widths (i.e., 128 bit and 256 bit port configurations; See Fig. 24).

Referring to claim 7, Yokoyama teaches a plurality of said input ports (e.g., ports for Processor Boards #1-#2 and Memory Boards #1-#2 in Fig. 1 configured as input ports, such that SW#2 being set '1' and SW#3 being set '1' make the port configure as an input port according to Figs. 3 and 11) are customized to have different width (i.e., 128 bit and 256 bit port configurations; See Fig. 24).

Referring to claim 8, Yokoyama teaches a plurality of said output ports (e.g., ports for DA I/O Board #1-#4 in Fig. 1 configured as output ports, such that SW#2 being set '0' and SW#3 being set '0' make the port configure as an output port according to Figs. 3 and 11) are customized to have different width (i.e., 128 bit and 256 bit port configurations; See Fig. 24).

Referring to claim 9, Yokoyama teaches said crossbar control data (i.e., discernment bits Sa and Sb, and Address in Fig. 2) contain control information for formatting bit length of data (i.e., control information for configuring 128 bit or 256 bit port; See Fig. 24) from an input port (e.g., port for Processor Boards #1-#2 and Memory Boards #1-#2 in Fig. 1 configured as an input port, such that SW#2 being set '1' and SW#3 being set '1' make the port configure as an input port according to Figs. 3 and 11) to be transmitted to an output port (e.g., port for DA I/O Board

#1-#4 in Fig. 1 configured as an output port, such that SW#2 being set '0' and SW#3 being set '0' make the port configure as an output port according to Figs. 3 and 11) with less width than said input port (e.g., 256 bit board → 128 bit board in Fig. 24; See Paragraph [0149]).

Referring to claim 11, Yokoyama discloses a crossbar (i.e., crossbar switching system in Fig. 1) having a plurality of paths for providing connections (i.e., a plurality of communication paths among Processor Boards #1-#2, Memory Boards #1-#2 and DA I/O Board #1-#4 in Fig. 1) between a plurality of ports (e.g., DA I/O Board #1-#4 in Fig. 1) and a plurality of system agents (e.g., Processor Boards #1-#2, and Memory Boards #1-#2 in Fig. 1) via a processing system (i.e., Crossbar Switch 5, Crossbar Switch I/O ports 6, Address Controller 8 and Data division 7 in Fig. 1) comprising: a plurality of ports (i.e., ports for Processor Boards #1-#2, Memory Boards #1-#2, and DA I/O Board #1-#4 in Fig. 1), each port capable of being an input port customized (See Figs. 3 and 11; i.e., SW#2 being set '1' and SW#3 being set '1' make the port customize as an input port in Fig. 3) for receiving data from a source agent (i.e., receiving data from Processor Board in Fig. 1) and an output port customized (See Figs. 3 and 11; i.e., SW#2 being set '0' and SW#3 being set '0' make the port customize as an output port in Fig. 3) for transferring data to a destination agent (i.e., transferring data to DA I/O port in Fig. 1); a plurality of virtual communication channels (i.e., data paths by the interconnection of switches in Fig. 5) on each input port (i.e., on each data division 7-1 of Fig. 6); and, crossbar control data (i.e., discernment bits Sa and Sb, and Address in Fig. 2) for specifying crossbar control information (i.e., Crossbar Switching control information) for transferring data from a virtual communication channel to an output port (See Figs. 25-38) having different port configurations (i.e., having 128 bit and 256 bit port configurations; See Paragraphs [0148], [0149], [0154], and [0155], as an example).

Referring to claim 12, Yokoyama discloses a method for transmitting data between customized ports (e.g., ports for DA I/O Board #1-#4 in Fig. 1 configured as output ports, such that SW#2 being set '0' and SW#3 being set '0' make the port configure as an output port

according to Figs. 3 and 11) and a plurality of system agents (e.g., Processor Boards #1-#2, and Memory Boards #1-#2 in Fig. 1) in a processing system via a crossbar (i.e., Crossbar Switch 5 of Fig. 1), wherein said crossbar includes a plurality of ports (i.e., ports for Processor Boards #1-#2, Memory Boards #1-#2, and DA I/O Board #1-#4 in Fig. 1), each port capable of being an input port customized (See Figs. 3 and 11; i.e., SW#2 being set '1' and SW#3 being set '1' make the port customize as an input port in Fig. 3) for receiving data from a source agent (i.e., receiving data from Processor Board in Fig. 1) and an output port customized (See Figs. 3 and 11; i.e., SW#2 being set '0' and SW#3 being set '0' make the port customize as an output port in Fig. 3) for transferring data to a destination agent (i.e., transferring data to DA I/O port in Fig. 1); and, crossbar control data (i.e., discernment bits Sa and Sb, and Address in Fig. 2) for specifying crossbar control information (i.e., Crossbar Switching control information) for transferring data from an input port to an output port (See Figs. 25-38) having different port configurations (i.e., having 128 bit and 256 bit port configurations; See Paragraphs [0148], [0149], [0154], and [0155], as an example), said method comprising the steps of: receiving data (See Box S1 in Fig. 12 and col. 15, lines 39-45) on an input port (e.g., port for Processor Board #1 of which both of SW#2 and SW#3 are set '1', i.e., making the port customize as an input port in Fig. 3); obtaining a destination output port (i.e., port configured as an output port, which is designated by Address in Fig. 1) for said data received on said input port (i.e., said received transfer request data including Data processed by Data division 7-1, 7-2, 7-3 and 7-4, and Address processed by Address Controller 8-1, 8-2, 8-3 and 8-4 in Fig. 1, respectively); determining whether said input port has the same configuration as said output port (See Decision Box S2 and Decision Box S6 in Fig. 12 and col. 15, lines 45-47 and col. 16, lines 7-11; i.e., determining whether said input port has 256 bit configuration as said output port having 256 bit configuration); obtaining control information from said crossbar control data when said input port does not have the same configurations as said output port (See Box S5 and Decision Box S6 in Fig. 12 and col. 16, lines

11-13); processing said data according to said obtained control information from said crossbar control data (See Box S12 in Fig. 12, Decision Box S18, Box S19 and S20 in Fig. 14 and paragraph [0094]); and, transmitting said processed data to said destination output port (See Box S21 in Fig. 14 and col. 17, lines 10-14).

Referring to claim 13, Yokoyama teaches reading control data received with said data on said input port (See Box S1 in Fig. 12 and col. 15, lines 41-45); determining whether said control data have valid port information (See Decision Box S2 in Fig. 12 and Decision Box S14 in Fig. 13 and paragraph [0098]; i.e., if a bit configuration information in said control data is not confirmed by OK from address line, then said control data has an invalid port information) and, aborting when said control data does not have valid port information (See Decision Box S16 and Box S17 in Fig. 13 and paragraph [0099]).

Referring to claim 15, Yokoyama teaches determining whether a width of said input port (See Decision Block S2 in Fig. 12; i.e., is the input port 256 bit configuration board ?) is more than a width of said output port (See Decision Block S6 in Fig. 12; e.g., if the communication partner is 128 bit configuration board); submitting said data as a processed data when said width of said input port is not more than said width of said output port (See Decision Box S2, Decision Box S6 and Box S9 in Fig. 12 and col. 15, lines 45-47 and col. 16, lines 7-11 and 14-20; i.e., determining whether said input port has 256 bit configuration as said output port having 256 bit configuration, and submitting 256 bit configured data as a processed data); obtaining said width of said output port when said width of said input port is greater than said width of said output port (See Decision Box S2, Decision Box S6 and Box S9 in Fig. 12 and col. 15, lines 45-47 and col. 16, lines 7-11 and 14-20; i.e., determining whether said input port has 256 bit configuration as said output port having 256 bit configuration, and obtaining 128 bit configured data width, for example); formatting said data from said input port to data configured for said obtained width of

said output port (See Box S20 in Fig. 14 and paragraphs [0090]-[0091]); and, submitting said formatted data as said processed data (See Box S21 in Fig. 14 and col. 17, lines 10-14).

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 2 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yokoyama [JP 411296473 A] as applied to claims 1, 3, 6-8, 11-13 and 15 above, and further in view of Applicant's Admitted Prior Art [hereinafter AAPA].

Referring to claim 2, Yokoyama discloses all the limitations of the claim 2 including said data received on said input port including control data for indicating destination information relating to data received on said input port (See paragraph [0080]), except that does not teach said data further comprising control data for indicating validity information relating to said data. AAPA discloses a crossbar (Fig. 1), wherein said crossbar using control information from control data, which indicates validity information relating to data received on an input port (See page 5, lines 13-16).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said validity information, as disclosed by AAPA, in said data received on said input port, as disclosed by Yokoyama, so as to verify the validity of port information relating to said data received on said input port, which is admitted by the applicant as well-known in the art (See AAPA, page 5, lines 13-19).

Referring to claim 14, Yokoyama discloses all the limitations of the claim 14 including obtaining said destination output port (i.e., port configured as an output port, which is designated

by Address in Fig. 1) from said control data (See paragraph [0080]), except that does not expressly teach said obtaining is performed when said control data has valid port information.

AAPA discloses a crossbar (Fig. 1), wherein obtaining a destination output port from said control data when said control data has valid port information (See page 5, lines 13-16).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said validity information, as disclosed by AAPA, in said data received on said input port, as disclosed by Yokoyama, so as to verify the validity of port information relating to said data received on said input port, which is admitted by the applicant as well-known in the art (See AAPA, page 5, lines 13-19).

9. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yokoyama [JP 411296473 A] as applied to claims 1, 3, 6-8, 11-13 and 15 above, and further in view of Tauchen et al. [US 6,411,230 B1; hereinafter Tauchen].

Referring to claim 4, Yokoyama discloses all the limitations of the claim 4 except that does not expressly teach at least one shift register on each input port for storing data in memory and shifting data with larger bit length to a smaller bit length data for transmission from an input port with more width to an output port with less width.

Tauchen discloses a circuit arrangement for parallel/serial conversion (See Abstract and Figure), wherein at least one shift register (i.e., first shift register 1 and second shift register 2 in Figure) on an input port for storing data in memory (See col. 3, lines 43-46) and shifting data with larger bit length to a smaller bit length data (See col.3, lines 62+; i.e., shifting D_{Pin} with larger parallel bit length to a smaller serial bit length D_{Sout} for Parallel/Serial conversion) for transmission from an input port with more width (i.e., a plurality of bits in parallel D_{Pin} in Figure) to an output port with less width (i.e., a serialized bits D_{Sout} in Figure).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said parallel/serial conversion, as disclosed by Tauchen, in said each

input port of said crossbar, as disclosed by Yokoyama, for the advantage of performing the conversion of said input data (e.g., 256 bit width data; i.e., parallel data) into (e.g., 1 bit width data in serial; i.e., serial data) without needing any external software or microprocessor control (See Tauchen, col. 4, line 66 through col. 5, line 8) in addition to the fixed bit width crossbar switching (i.e., crossbar switching between 256 bit width and 128 bit width; See Yokoyama, Figs. 1 and 24).

10. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yokoyama [JP 411296473 A] as applied to claims 1, 3, 6-8, 11-13 and 15 above, and further in view of Aimoto [US 6,570,876 B1].

Referring to claim 5, Yokoyama discloses all the limitations of the claim 5 except that does not expressly teach at least one multiplexor device on each said input port and each said output port for prioritizing transmissions of data.

Aimoto discloses a packet switch and switching method (See col. 1, lines 8-16 and Fig. 1), wherein at least one multiplexor device (i.e., relaying priority control unit 3 and received packet queuing unit 7 of input port interface 20 in Fig. 1, and transmission priority control unit 5 and transmission packet queuing unit 8 of output port interface 21 in Fig. 1) on each input port (i.e., input port interface 20 of Fig. 1) and each output port (i.e., output port interface 21 of Fig. 1) for prioritizing transmissions of data (See col. 5, line 42 through col. 6, line 46).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said multiplexor device, as disclosed by Aimoto, in said each input port of said crossbar, as disclosed by Yokoyama, for the advantage of providing crossbar switching (i.e., packet switching) that can perform both bandwidth control and priority control according to the communication protocol of variable length data (i.e., packet; See Aimoto, col. 2, lines 23-26).

11. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yokoyama [JP 411296473 A] as applied to claims 1, 3, 6-8, 11-13 and 15 above, and further in view of Hsieh et al. [US 5,717,871 A; cited by the Applicant; hereinafter Hsieh].

Referring to claim 10, Yokoyama discloses all the limitations of the claim 10 except that does not expressly teach said crossbar control data contain control information for use by any one from the group of a shift register or a multiplexor device.

Hsieh discloses a programmable port for crossbar switch 10 in Fig. 1, wherein said programmable port receiving crossbar control data (See col. 9, lines 34-36) contain control information (See col. 9, lines 39-41) for use by any one from the group of a shift register (i.e., shift register 20 of Fig. 5).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have implemented said programmable port, as disclosed by Hsieh, on said each port of said crossbar, as disclosed by Yokoyama, for the advantage of providing a port flexibility in the use of control inputs and reduces the number of crossbar switch control inputs required to implement various modes of port operation (See Hsieh, col. 2, lines 43-49).

12. Claims 16 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yokoyama [JP 411296473 A] in view of what was well known in the art, as exemplified by Lach [US 6,363,452 B1].

Referring to claim 16, Yokoyama discloses a system (i.e., crossbar switching system including in Fig. 1) for transmitting data between customized ports (e.g., ports for DA I/O Board #1-#4 in Fig. 1 configured as output ports, such that SW#2 being set '0' and SW#3 being set '0' make the port configure as an output port according to Figs. 3 and 11) and a plurality of system agents (e.g., Processor Boards #1-#2, and Memory Boards #1-#2 in Fig. 1) in a processing system via a crossbar (i.e., Crossbar Switch 5 of Fig. 1), wherein said crossbar includes a plurality of ports (i.e., ports for Processor Boards #1-#2, Memory Boards #1-#2, and DA I/O Board #1-#4 in

Fig. 1), each port capable of being an input port customized (See Figs. 3 and 11; i.e., SW#2 being set '1' and SW#3 being set '1' make the port customize as an input port in Fig. 3) for receiving data from a source agent (i.e., receiving data from Processor Board in Fig. 1) and an output port customized (See Figs. 3 and 11; i.e., SW#2 being set '0' and SW#3 being set '0' make the port customize as an output port in Fig. 3) for transferring data to a destination agent (i.e., transferring data to DA I/O port in Fig. 1), and crossbar control data (i.e., discernment bits Sa and Sb, and Address in Fig. 2) for indicating crossbar control information (i.e., Crossbar Switching control information) for transmitting data from an input port to an output port (See Figs. 25-38) having different port configurations (i.e., having 128 bit and 256 bit port configurations; See Paragraphs [0148], [0149], [0154], and [0155], as an example), comprising: a storage medium (i.e., memory A 61b-1, and memory B 61c-1 in Fig. 9); a machine (i.e., means for switching in crossbar switch 5 of Fig. 1 for executing the flows in Figs. 12-15 and 17-23) for transmitting data between customized ports (e.g., ports for DA I/O Board #1-#4 in Fig. 1 configured as output ports, such that SW#2 being set '0' and SW#3 being set '0' make the port configure as an output port according to Figs. 3 and 11) and a plurality of system agents (e.g., Processor Boards #1-#2, and Memory Boards #1-#2 in Fig. 1) in a processing system via a crossbar (i.e., Crossbar Switch 5 of Fig. 1), said machine comprising a set of flow steps for: receiving data (See Box S1 in Fig. 12 and col. 15, lines 39-45) on an input port (e.g., port for Processor Board #1 of which both of SW#2 and SW#3 are set '1', i.e., making the port customize as an input port in Fig. 3); obtaining a destination output port (i.e., port configured as an output port, which is designated by Address in Fig. 1) for said data received on said input port (i.e., said received transfer request data including Data processed by Data division 7-1, 7-2, 7-3 and 7-4, and Address processed by Address Controller 8-1, 8-2, 8-3 and 8-4 in Fig. 1, respectively); determining whether said input port has the same configuration as said output port (See Decision Box S2 and Decision Box S6 in Fig. 12 and col. 15, lines 45-47 and col. 16, lines 7-11; i.e., determining whether said input port has 256

bit configuration as said output port having 256 bit configuration); obtaining control information from said crossbar control data when said input port does not have the same configurations as said output port (See Box S5 and Decision Box S6 in Fig. 12 and col. 16, lines 11-13); processing said data according to said obtained control information from said crossbar control data (See Box S12 in Fig. 12, Decision Box S18, Box S19 and S20 in Fig. 14 and paragraph [0094]); and, transmitting said processed data to said destination output port (See Box S21 in Fig. 14 and col. 17, lines 10-14).

Yokoyama does not expressly teach said machine comprising a set of instructions for said flow steps.

The Examiner takes Official Notice that said flow steps could be achieved in all software implementation (i.e., instructions) with the same or equivalent results, using appropriate program codes (i.e., processor instructions), is well known to one of ordinary skill in the art, as evidenced by Lach, at col. 12, lines 3-9.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to have implemented said flow steps , as disclosed by Yokoyama, in software since it would allow a better flexibility of an implementation than a hardware implementation.

Referring to claim 17, Yokoyama discloses a machine (i.e., means for switching in crossbar switch 5 of Fig. 1 for executing the flows in Figs. 12-15 and 17-23) for transmitting data between customized ports (e.g., ports for DA I/O Board #1-#4 in Fig. 1 configured as output ports, such that SW#2 being set '0' and SW#3 being set '0' make the port configure as an output port according to Figs. 3 and 11) and a plurality of system agents (e.g., Processor Boards #1-#2, and Memory Boards #1-#2 in Fig. 1) in a processing system via a crossbar (i.e., Crossbar Switch 5 of Fig. 1), said machine comprising a set of flow steps to: receive data (See Box S1 in Fig. 12 and col. 15, lines 39-45) on an input port (e.g., port for Processor Board #1 of which both of SW#2 and SW#3 are set '1', i.e., making the port customize as an input port in Fig. 3); obtain a

destination output port (i.e., port configured as an output port, which is designated by Address in Fig. 1) for said data received on said input port (i.e., said received transfer request data including Data processed by Data division 7-1, 7-2, 7-3 and 7-4, and Address processed by Address Controller 8-1, 8-2, 8-3 and 8-4 in Fig. 1, respectively); determine whether said input port has the same configuration as said output port (See Decision Box S2 and Decision Box S6 in Fig. 12 and col. 15, lines 45-47 and col. 16, lines 7-11; i.e., determining whether said input port has 256 bit configuration as said output port having 256 bit configuration); obtain control information from a crossbar control data when said input port does not have the same configurations as said output port (See Box S5 and Decision Box S6 in Fig. 12 and col. 16, lines 11-13); process said data according to said obtained control information from said crossbar control data (See Box S12 in Fig. 12, Decision Box S18, Box S19 and S20 in Fig. 14 and paragraph [0094]); and, transmit said processed data to said destination output port (See Box S21 in Fig. 14 and col. 17, lines 10-14). Yokoyama does not expressly teach said machine comprising a set of instructions for said flow steps.

The Examiner takes Official Notice that said flow steps could be achieved in all software implementation (i.e., instructions) with the same or equivalent results, using appropriate program codes (i.e., processor instructions), is well known to one of ordinary skill in the art, as evidenced by Lach, at col. 12, lines 3-9.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to have implemented said flow steps , as disclosed by Yokoyama, in software since it would allow a better flexibility of an implementation than a hardware implementation.

Conclusion

13. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

With regard to Crossbar Switching,

Kothary [US 6,249,528 B1] discloses network switch providing per virtual channel queuing for segmentation and reassembly.

Vu [US 2002/0186656 A1] discloses automatic load balancing in switch fabric.

Aguilar et al. [US 6,324,613 B1] disclose port router.

Hirata [JP 411265341 A] discloses input/output bus bridge device.

With regard to Bit Width Controlling,

Hasegawa [US 5,941,941 A] discloses bit width controlling method.

With regard to Bus Decoupling,

Rutman [US 5,313,586 A] discloses co-process de-coupling bus structure.

14. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christopher E. Lee whose telephone number is 703-305-5950. The examiner can normally be reached on 9:00am - 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark H. Rinehart can be reached on 703-305-4815. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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